

What is claimed is:

[Claim 1] 1. An electrostatic discharge protection device with positive voltage and negative voltage tolerance, the device being connected to a pad in an integrated circuit, the device comprising:

a first type substrate;

a first type well, disposed inside the first type substrate, the first type well being in a floating state;

a second type well, disposed inside the first type substrate, the second type well separating the first type well from the first type substrate, the second type well being coupled to a first voltage line;

a second type first doped region, disposed inside the first type well, the second type first doped region being coupled to a second voltage line;

a second type second doped region, disposed inside the first type well and coupled to the pad; and

an isolation structure between the second type first doped region and the second type second doped region.

[Claim 2] 2. The device of claim 1, wherein the first type is a P type and the second type is an N type.

[Claim 3] 3. The device of claim 1, wherein the second type well comprises a deep second type well.

[Claim 4] 4. The device of claim 1, wherein the second type well comprises a second type buried layer and a high voltage second type well.

[Claim 5] 5. The device of claim 1, wherein the isolation structure is a field oxide region.

[Claim 6] 6. The device of claim 1, wherein the isolation structure is a shallow trench isolation region.

[Claim 7] 7. The device of claim 1, wherein a voltage of the first voltage line is a system voltage, and a voltage of the second voltage line is a ground voltage.

[Claim 8] 8. The device of claim 1, wherein a voltage of the first voltage line and a voltage of the second voltage line are system voltages.

[Claim 9] 9. The device of claim 1, wherein a voltage of the first voltage line and a voltage of the second voltage line are ground voltage.

[Claim 10] 10. An electrostatic discharge protection device with positive voltage and negative voltage tolerance, for protecting an internal circuit in an integrated circuit, the internal circuit comprising at least a positive voltage input/output terminal and a negative voltage input/output terminal, the device comprising:

a first type substrate;

a first type first well, disposed inside the first type substrate, the first type first well being in a floating state;

a second type first well, disposed inside the first type substrate, the second type first well separating the first type first well from the first type substrate, the second type first well being coupled to a system voltage line;

a second type first doped region, disposed inside the first type first well and coupled to the system voltage line;

a second type second doped region, disposed inside the first type first well and coupled to the positive voltage input/output terminal;

a first isolation structure, disposed between the second type first doped region and the second type second doped region;
a first type second well, disposed inside the first type substrate, the first type second well being in a floating state;
a second type second well, disposed inside the first type substrate separating the first type second well from the first type substrate, the second type second well being coupled to a ground voltage line;
a second type third doped region, disposed inside the first type second well, the second type third doped region being coupled to the ground voltage line;
a second type fourth doped region, disposed inside the first type second well and coupled to the negative voltage input/output terminal; and
a second isolation structure between the second type third doped region and the second type fourth doped region.

[Claim 11] 11. The device of claim 10, wherein the first type is a P type and the second type is an N type.

[Claim 12] 12. The device of claim 10, wherein each of the second type first well and the second type second well comprises a deep second type well.

[Claim 13] 13. The device of claim 10, wherein each of the second type first well and the second type second well comprises a second type buried layer and a high voltage second type well.

[Claim 14] 14. The device of claim 10, wherein each of the first isolation structure and the second isolation structure is a field oxide region.

[Claim 15] 15. The device of claim 10, wherein each of the first isolation structure and the second isolation structure is a shallow trench isolation region.